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**Han**

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(54) **SEMICONDUCTOR LIGHT EMITTING  
DEVICE AND METHOD OF FABRICATING  
THE SAME**

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See application file for complete search history.

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(52) **U.S. Cl.**

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(57) **ABSTRACT**

A semiconductor light emitting device comprises a first  
electrode contacting layer, a first active layer on the first  
electrode contacting layer, a second electrode contacting  
layer on the first active layer, a second active layer on the  
second electrode contacting layer, and a third electrode  
contacting layer on the second active layer.

(58) **Field of Classification Search**

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Fig. 1

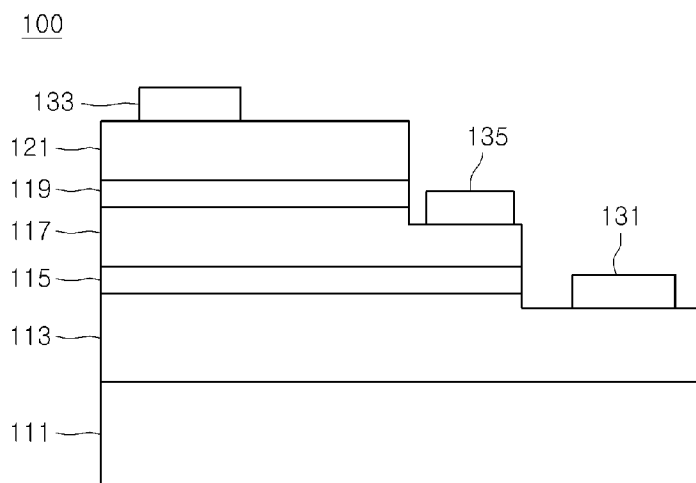


Fig. 2

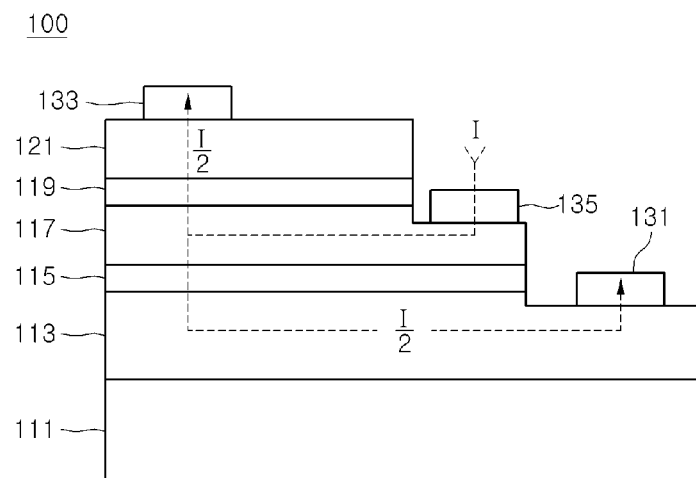


Fig. 3

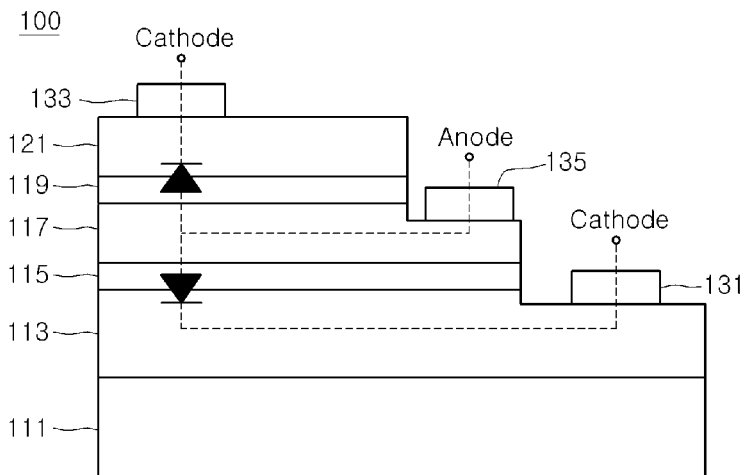


Fig. 4

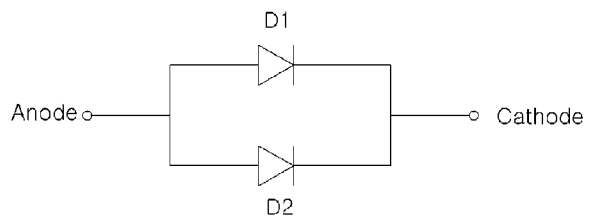


Fig. 5

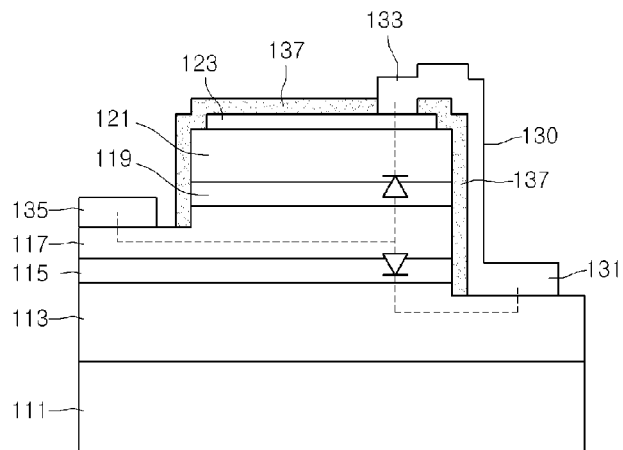


Fig. 6

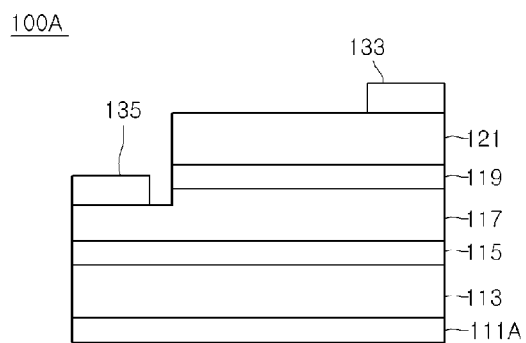


Fig. 7

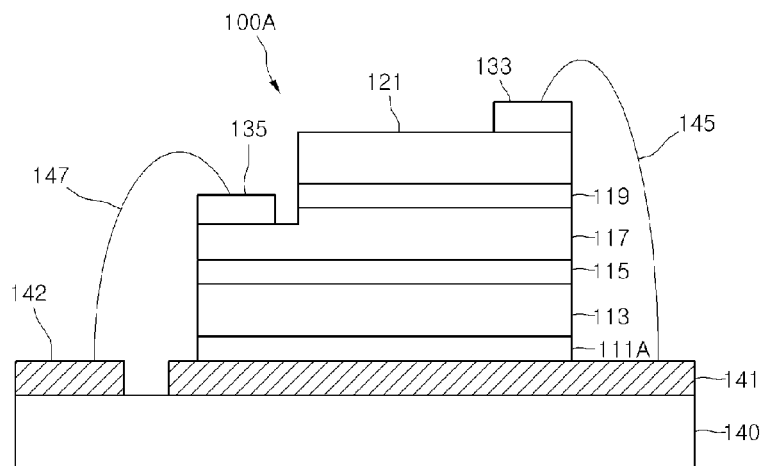


Fig. 8

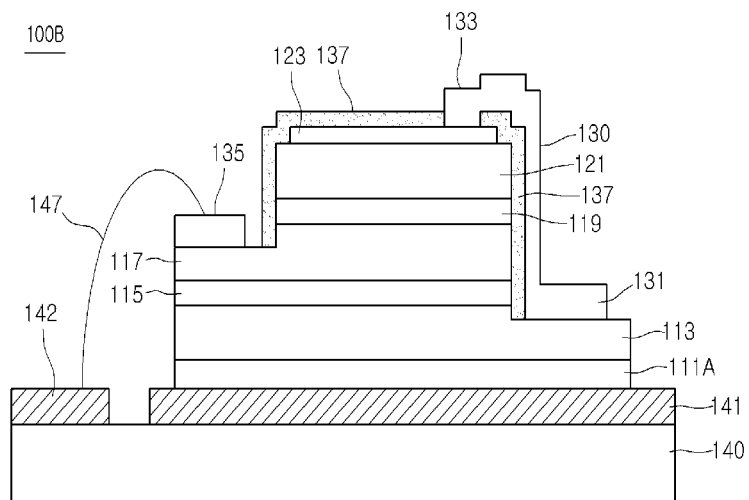


Fig. 9

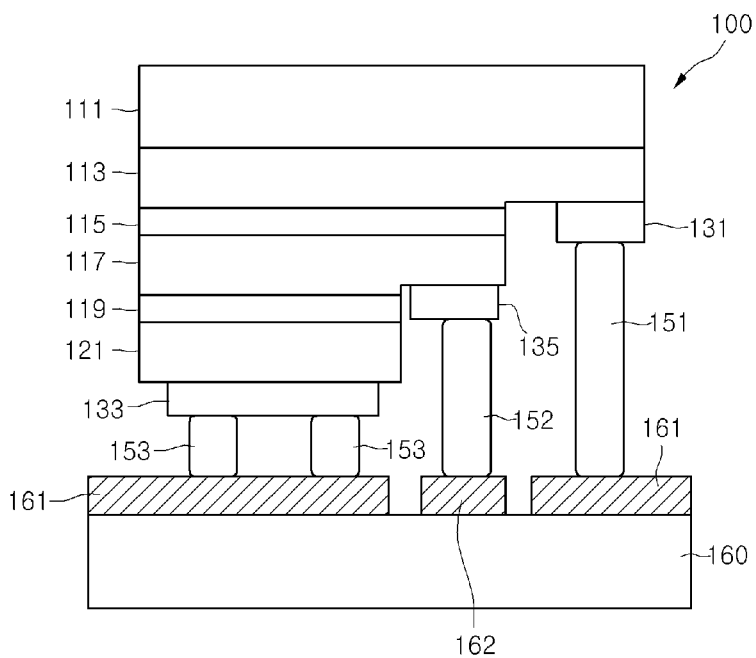


Fig. 10



Fig. 11



Fig. 12

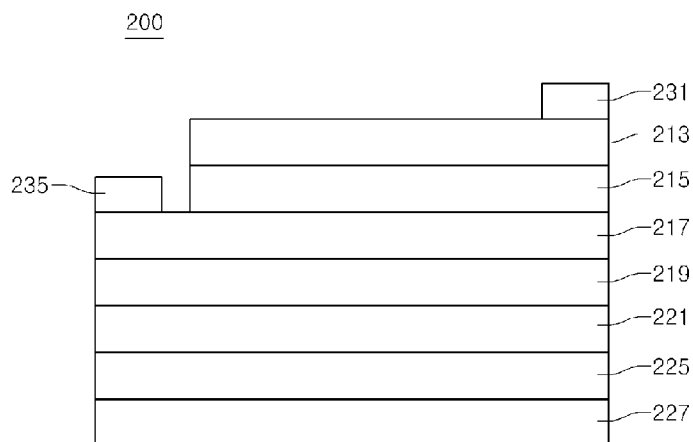


Fig. 13

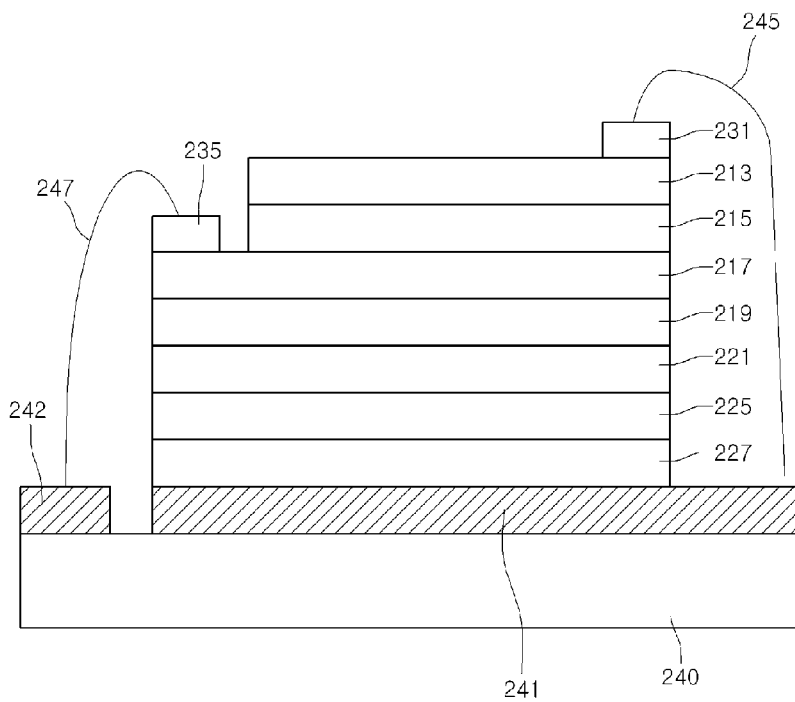
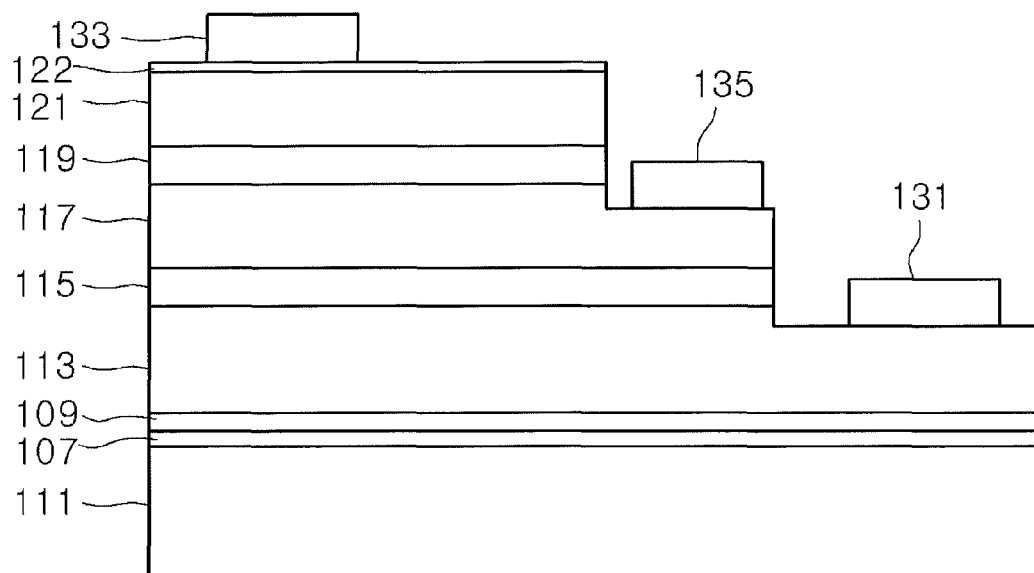


FIG. 14



1

# SEMICONDUCTOR LIGHT EMITTING DEVICE AND METHOD OF FABRICATING THE SAME

## TECHNICAL FIELD

The present disclosure relates to a semiconductor light emitting device and a method of fabricating the same.

## BACKGROUND ART

Light emitting diode (LED) can emit light with a variety of colors using properties of compound semiconductor materials such as a GaAs-based compound, an AlGaAs-based compound, a GaN-based compound, an InGaN-based material, and an InGaAlP-based material. The light emitting diodes are packaged and used as light sources in a variety of fields such as a lightening display field, a character display field, and an image display field.

## DISCLOSURE OF INVENTION

### Technical Problem

Embodiments provide a semiconductor light emitting device that is designed to emit light through a plurality of active layers and a method of fabricating the same.

Embodiments provide a semiconductor light emitting device that is designed to enlarge an effective light emitting area using a plurality of active layers.

### Technical Solution

An embodiment provides a semiconductor light emitting device comprising: a first electrode contacting layer, a first active layer on the first electrode contacting layer, a second electrode contacting layer on the first active layer, a second active layer on the second electrode contacting layer, and a third electrode contacting layer on the second active layer.

An embodiment provides a semiconductor light emitting device comprising: a plurality of first electrode contacting layers spaced apart from each other, a second electrode contacting layer between the first electrode contacting layers, a plurality of active layers between the first and second electrode contacting layers, and a first electrode electrically connected to the first electrode contacting layers.

An embodiment provides a method of fabricating a semiconductor light emitting device comprising: forming a first electrode contacting layer, forming a first active layer on the first electrode contacting layer, forming a second electrode contacting layer on the first active layer, forming a second active layer on the second electrode contacting layer, and forming a third electrode contacting layer on the second active layer.

### Advantageous Effects

According to the embodiments, the effective light emitting area can be enlarged as compared to a chip size of the semiconductor light emitting device.

In addition, a density of a current supplied to the semiconductor light emitting device can be reduced, the efficiency of the light emitting device can be improved.

Further, the reliability of the semiconductor light emitting device can be improved.

The details of one or more embodiments are set forth in the accompanying drawings and the description below.

2

Other features will be apparent from the description and drawings, and from the claims.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of a semiconductor light emitting device according to a first embodiment.

FIG. 2 is a schematic view illustrating a current path of FIG. 1.

FIG. 3 is a schematic view of a semiconductor light emitting device according to a first embodiment.

FIG. 4 is a circuit diagram of a light emitting diode of FIG. 3.

FIG. 5 is a schematic view of a semiconductor light emitting device according to a second embodiment.

FIG. 6 is a schematic view of a semiconductor light emitting device according to a third embodiment.

FIG. 7 is a schematic view illustrating mounting of the semiconductor light emitting device of FIG. 6.

FIG. 8 is a schematic view illustrating mounting of a semiconductor light emitting device according to a fourth embodiment.

FIG. 9 is a schematic view illustrating flip-type mounting of the semiconductor light emitting device according to the first embodiment.

FIGS. 10 to 12 are cross-sectional views illustrating a method of fabricating a semiconductor device according to a fifth embodiment.

FIG. 13 is a schematic view of mounting of a semiconductor light emitting device according to the fifth embodiment.

FIG. 14 is a schematic view of mounting of a semiconductor light emitting device according to a sixth embodiment.

## BEST MODE FOR CARRYING OUT THE INVENTION

Hereinafter, semiconductor light emitting devices in accordance with embodiments will be described with reference to the accompanying drawings. Reference will now be made in detail to the embodiments of the present disclosure, examples of which are illustrated in the accompanying drawings. In the following description, words "above", "on", "below", and "under" are based on the accompanying drawings. In addition, a thickness of each layer is only exemplarily illustrated in the drawings and is not limited to the drawing.

FIG. 1 is a cross-sectional view of a semiconductor light emitting device according to a first embodiment.

Referring to FIG. 1, a semiconductor light emitting device 100 comprises a substrate 111, a first electrode contacting layer 113, a first active layer 115, a second electrode contacting layer 117, a second active layer 119, a third electrode contacting layer 121, first electrodes 131 and 133, and a second electrode 135.

The substrate 111 may be formed of one selected from the group consisting of a sapphire ( $\text{Al}_2\text{O}_3$ ) substrate, a GaN substrate, a SiC substrate, a ZnO substrate, a Si substrate, a GaP substrate, a substrate containing metal, or a conductive substrate.

A buffer layer 107 is formed on the substrate 111. The buffer layer may be formed of at least one of GaN, AlN, AlGaIn, InGaIn, and AlGaInN. An undoped semiconductor layer 109 may be formed on the substrate 111 or the buffer layer 107. The undoped semiconductor layer 109 may be formed of undoped GaN, as depicted in FIG. 14.



The first electrode contacting layer **113** is formed on the substrate **111**. The first electrode contacting layer **113** comprises at least one n-type semiconductor layer and doped with n-type dopants. The n-type semiconductor layer may be formed of a compound semiconductor material selected from the group consisting of GaN, InN, AlN, InGaN, AlGaIn, InAlGaIn, AlInN, and a combination thereof. The n-type dopants comprise IV group elements such as Si, Ge, Sn, Se, Te, and the like.

The first active layer **115** is formed on the first electrode contacting layer **113**. The first active layer **115** may be formed in a single quantum well structure or a multi-quantum well structure. The first active layer **115** is formed of a material having a band gap energy in accordance with a wavelength of light emitted. For example, for blue light-emitting having a wavelength of 460-470nm, the first active layer **115** may be formed of the single quantum well structure or a multi-quantum well structure with one cycle of an InGaIn well layer/GaN barrier layer. Here, the  $\text{In}_x\text{Ga}_{1-x}\text{N}$  well layer may be adjusted to satisfy the following:  $0 \leq x \leq 1$ . The first active layer **115** may comprise a material emitting colored light such as light having a blue wavelength, light having a red wavelength, and light having a green wavelength.

The second electrode contacting layer **117** is formed on the first active layer **115**. The second electrode contacting layer **117** comprises at least one p-type semiconductor layer and doped with p-type dopants. The p-type semiconductor layer may be formed of a compound semiconductor material selected from the group consisting of GaN, InN, AlN, InGaIn, AlGaIn, InAlGaIn, AlInN, and a combination thereof. The p-type dopants comprise a II group element such as Mg, Zn, Ca, Sr, Ba, and the like.

The second active layer **119** is formed on the second electrode contacting layer **117**. The second active layer **119** is formed of a same material as the first active layer **115**. For example, the second active layer **119** may be grown as an InGaIn well layer/GaN barrier layer structure. However, a material for the first and second active layers **115** and **119** are not specifically limited. That is, the material for the first and second active layers **115** and **119** may vary in accordance with the wavelength of light that will be emitted. Growing cycles of the well layer/barrier layer structures of the respective first and second active layers **115** and **119** may be same as or different from each other.

In addition, a clad layer (not shown) may be formed on or underneath the first and/or second active layers **115** and **119**. The clad layer may be an AlGaIn layer. However, the present disclosure is not limited to this.

The third electrode contacting layer **121** is formed on the second active layer **119**. The third electrode contacting layer **121** comprises at least one n-type semiconductor layer and doped with n-type dopants. The n-type semiconductor layer may be formed of a compound semiconductor material selected from the group consisting of GaN, InN, AlN, InGaIn, AlGaIn, InAlGaIn, AlInN, and a combination thereof. The n-type dopants comprise IV group elements such as Si, Ge, Sn, Se, Te, and the like. Here, as the word "third electrode contacting layer **121**" is just for the descriptive convenience, it has a same function as the first electrode contacting layer **113**.

A transparent electrode layer (not shown) may be formed on the third electrode contacting layer **121**.

The materials for the respective first and third electrode contacting layers **113** and **121** may be same as or different from each other. However, the present disclosure is not limited to this. The first and third electrode contacting layers

**113** and **121** may be the n-type semiconductor layers while the second electrode contacting layer **117** is the p-type semiconductor layer. Alternatively, The first and third electrode contacting layers **113** and **121** may be the p-type semiconductor layers while the second electrode contacting layer **117** is the n-type semiconductor layer. In addition, a thin n-type or p-type semiconductor layer **122** may be formed on the third electrode contacting layer **121**, as depicted in FIG. **14**.

After the third electrode contacting layer **121** or the transparent electrode is formed, a MESA etching process is performed to expose a part of the first electrode contacting layer **113** and a part of the second electrode contacting layer **117**. The first electrodes **131** and **133** are formed on the respective first and third electrode contacting layers **113** and **121**. The second electrode **135** is formed on the second electrode contacting layer **117**. One of the first electrodes **131** and **133** may be omitted.

The first electrodes **131** and **133** may be formed of a material selected from the group consisting of Ti, Al, In, Ta, Pd, Co, Ni, Si, Ge, Ag, Au, and a combination thereof. Each of the first electrodes **131** and **133** may be a single layer structure or a multi-layer structure. However, the present disclosure is not limited to this. The second electrode **135** may be formed of a material selected from the group consisting of Ag, Ag alloy, Ni, Al, Al alloy, Rh, Pd, Ir, Ru, Mg, Zn, Pt, Au, Hf, and a combination thereof. The second electrode **135** may be a single layer structure or a multi-layer structure. However, the present disclosure is not limited to this.

Here, the first electrodes **131** and **133** formed on the respective first and third electrode contacting layers **113** and **121** may be interconnected by a wire or a conductive thin film.

The semiconductor light emitting device **100** comprises the plurality of active layers **115** and **119** and thus the effective light emitting area is enlarged by two times as compared to a same size chip.

FIG. **2** is a schematic view illustrating a current path of FIG. **1**, and FIG. **3** is a schematic view of a semiconductor light emitting device according to a first embodiment.

Referring to FIG. **2**, when a current **I** is supplied to the electrodes **131**, **135**, and **133**, half of the current **I** supplied to the second electrode contacting layer **117** is transferred to the first electrode contacting layer **113** through the first active layer **115** and the other half of the current **I** is transferred to the third electrode contacting layer **121** through the second active layer **119**. As a result, the semiconductor light emitting device **100** can be driven with a less operational voltage that an existing device even when a same current as the existing device is supplied while a similar intensity of the light is output.

In addition, in the semiconductor light emitting device **100**, the current density is reduced by half and the operational voltage is reduced, thereby improving the luminance efficiency. At this point, the intensity of the light is the same as the existing device.

FIG. **3** is a schematic view of a semiconductor light emitting device according to a first embodiment, and FIG. **4** is a circuit diagram of a light emitting diode of FIG. **3**.

Referring to FIGS. **3** and **4**, the semiconductor light emitting device **100** is structured such that the second electrode contacting layer **117** is disposed between the first and third electrode contacting layers **113** and **121** and the first and second active layers **115** and **119** are disposed between the first and third electrode contacting layers **113** and **121**. Therefore, the first electrode contacting layer **113**,

5

the first active layer **115**, and the second electrode contacting layer **117** formed a first light emitting diode CHEN and the third electrode contacting layer **121**, the second active layer **119**, and the second electrode contacting layer **117** formed a second light emitting diode SHIM.

The first and second light emitting diodes **D1** and **D2** may be arranged in parallel in terms of a circuit structure.

The first electrodes **131** and **133** on the respective first and third electrode contacting layers **113** and **121** may function as cathodes that are commonly connected. The second electrode **135** on the second electrode contacting layer **117** may function as an anode.

FIG. **5** is a schematic view of a semiconductor light emitting device according to a second embodiment. In the following description, same parts as those of the first embodiment will refer to the first embodiment and detailed description thereof will be omitted.

Referring to FIG. **5**, a transparent electrode layer **123** may be formed on the third electrode contacting layer **121**. The transparent electrode layer **123** is a transparent oxide layer that is formed to enhance the diffusion of the current on an entire surface of the chip. The transparent electrode may be formed of ITO, ZnO, RuOx, TiOx, IrOx, and the like.

A part of the first electrode contacting layer **113** and a part of the second electrode contacting layer **117** are exposed through a MESA etching process. Here, electrode forming regions may be formed by etching insulating layers **137** formed on a surface of the semiconductor layer. Alternatively, the insulating layers **137** may be formed on the surface of the semiconductor layer except for the electrode forming regions. That is, the electrode forming method is not specifically limited.

The first electrodes **131** and **133** are formed on the first electrode contacting layer **113** and the transparent electrode layer **123**, respectively. The second electrode **135** is formed on the second electrode contacting layer **117**. Here, the first electrode **133** may be formed on the third electrode contacting layer **121**.

The first electrode **131** on the first electrode contacting layer **113** and the first electrode **133** on the transparent electrode layer **123** may be interconnected by an electrode connecting layer **130**. The electrode connecting layer **130** is formed on the insulating layer **137** to be electrically insulated from other semiconductor layers. Here, the electrodes **131** and **133**, the electrode connecting layer **130**, and the insulating layers **137** may be grown through a PECVD or sputtering process. However, the present disclosure is not limited to this.

FIG. **6** is a schematic view of a semiconductor light emitting device according to a third embodiment. In the following description, same parts as those of the first embodiment will refer to the first embodiment and detailed description thereof will be omitted.

Referring to FIG. **6**, a vertical type semiconductor light emitting device **100A** is structured to have a conductive substrate **111A** at its lower portion. The conductive substrate **111A** may be formed after removing the substrate **111** of FIG. **1** or by making the substrate **111** of FIG. **1** conductive. The removal of the substrate may be realized through a laser lift off (LLO) process.

The conductive substrate **111A** is provided to support a light emitting diode chip. The conductive substrate **111A** may be formed of Si or Mo and attached to the device. Alternatively, the conductive substrate **111A** may be formed by thickly plating Cu.

6

Since the conductive substrate **111A** is electrically connected to the first electrode contacting layer **113**, there is no need to form the first electrode or to perform the MESA etching process.

FIG. **7** is a schematic view illustrating mounting of the semiconductor light emitting device of FIG. **6**.

Referring to FIG. **7**, the vertical type semiconductor light emitting device **100A** is mounted on a sub-mount **140**. The sub-mount **140** may be a semiconductor substrate formed of SiC, GaN, GaAs, Si, and the like, a lead frame type support, an electroplating type support, or a normal PCB, a flexible PCB. However, the present disclosure is not limited to this configuration.

The conductive substrate **111A** is attached on a first electrode pad **141** of the sub-mount **140** by conductive adhesive. The first electrode **133** on the third electrode contacting layer **121** is connected to the first electrode pad **141** of the sub-mount **140** by a wire **145**.

The second electrode **135** on the second electrode contacting layer **117** may be connected to the second electrode pad **142** of the sub-mount **140** by a wire **147**.

FIG. **8** is a schematic view illustrating mounting of a semiconductor light emitting device according to a fourth embodiment. In the following description, same parts as those of the second embodiment will refer to the second embodiment and detailed description thereof will be omitted.

Referring to FIG. **8**, a semiconductor light emitting device **100B** is structured to have a conductive substrate **111A** at its lower portion, and structured to be mounted on a sub-mount by one wire **147**. The conductive substrate **111A** is attached on the first electrode pad **141** of the sub-mount **140** by the conductive adhesive so that the first electrode pad **141** can be electrically connected to the first electrode contacting layer **113**. The first electrode **131** on the first electrode contacting layer **113** is electrically connected to the first electrode **133** on the transparent electrode layer **123** through the electrode connecting layer **130**.

The second electrode **135** of the second electrode contacting layer **117** is connected to the second electrode pad **142** of the sub-mount by the wire **147**.

The third electrode contacting layer **121** is connected to the first electrode **133** through the transparent electrode layer **123**, the first electrodes **131** and **133** are connected through the electrode connecting layer **130**, the conductive substrate **111A** is connected to the first electrode **131** through the first electrode connecting layer **113**, and the first electrode pad **141** is connected to the conductive substrate **111A**.

FIG. **9** is a schematic view illustrating flip-type mounting of the semiconductor light emitting device according to the first embodiment.

Referring to FIG. **9**, the first electrode **131** of the semiconductor light emitting device **100** is connected to a first electrode pad **161** of a sub-mount **160** by a first bump (e.g., Au bump) **151**. The second electrode **135** is connected to a second electrode pad **162** of the sub-mount **160** by a second bump **152**. The first electrode **133** is connected to the first electrode pad **161** of the sub-mount **160** by a third bump **153**.

FIGS. **10** to **12** are cross-sectional views illustrating a method of fabricating a semiconductor device according to a fifth embodiment. In the following description, component parts of the fifth embodiment which are the same as those of the first embodiment are not described.

Referring to FIG. **10**, a first electrode contacting layer **213** is formed on a substrate **211** and a first active layer **215** is formed on the first electrode contacting layer **213**. A second electrode contacting layer **217** is formed on the first active

layer **215**. A second active layer **219** is formed on the second electrode contacting layer **217** and a third electrode contacting layer **221** is formed on the second active layer **219**. A variety of other layers such as a buffer layer or/and an undoped GaN layer may be formed between the substrate **211** and the first electrode contacting layer **213**.

Referring to FIG. **11**, a reflective electrode layer **225** is formed on the third electrode contacting layer **221** and a conductive supporting member **227** is formed on the reflective electrode layer **225**. The reflective electrode layer **225** comprises Al, Ag, Pd, Rh, Pt, and the like. The conductive supporting member **227** may be formed of copper or gold. However, the present disclosure is not limited to this.

Referring to FIGS. **11** and **12**, the substrate **121** is removed through the LLO process and the conductive supporting member **227** is located on the base. Here, the variety of other layers formed between the substrate **121** and the first electrode contacting layer **213** may be removed through a dry or wet etching process.

After the above, a part of the second electrode contacting layer **217** is exposed through a MESA etching process. A second electrode **235** is formed on the second electrode contacting layer **217** and a first electrode **231** is formed on the first electrode contacting layer **213**.

FIG. **13** is a schematic view of mounting of a semiconductor light emitting device according to the fifth embodiment.

Referring to FIG. **13**, the first electrode **231** is connected to a first electrode pad **241** of a sub-mount **240** by a wire **245** and the second electrode **235** is connected to a second electrode pad **242** of the sub-mount by a wire **247**.

According to the semiconductor light emitting device of the embodiment, the light emitting area can be enlarged by forming the plurality of active layers. That is, the effective area of the light emitting region can be enlarged in the same LED chip. In addition, the current density is reduced to improve the luminance efficiency.

In addition, each layer of the semiconductor light emitting device of the embodiment comprises a compound semiconductor using elements of III-V group. For example, the layers may be formed of a GaN-based, GaAs-based, InGaAlP-based, or AlGaAs-based material.

In the following description, it will be understood that when a layer (or film) is referred to as being on another layer or substrate, it can be directly on the another layer or substrate, or intervening layers may also be present. Further, it will be understood that when a layer is referred to as being under another layer, it can be directly under the another layer, and one or more intervening layers may also be present. In addition, it will also be understood that when a layer is referred to as being between two layers, it can be the only layer between the two layers, or one or more intervening layers may also be present.

Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

## INDUSTRIAL APPLICABILITY

According to the embodiments, the effective light emitting area can be enlarged as compared to a chip size of the semiconductor light emitting device.

In addition, a density of a current supplied to the semiconductor light emitting device can be reduced, the efficiency of the light emitting device can be improved.

Further, the reliability of the semiconductor light emitting device can be improved.

The invention claimed is:

1. A semiconductor light emitting device, comprising:
  - a first electrode contacting layer including a p-type dopant;
  - a first active layer on the first electrode contacting layer;
  - a second electrode contacting layer on the first active layer and including an n-type dopant;
  - a second active layer on the second electrode contacting layer;
  - a third electrode contacting layer on the second active layer and including a p-type dopant;
  - a first electrode on a region of a top surface of the third electrode contacting layer;
  - a second electrode on a region of a top surface of the second electrode contacting layer;
  - a reflective electrode layer disposed under the first electrode contacting layer;
  - a conductive support member disposed under the reflective electrode layer;
  - a first electrode pad under the conductive support member;
  - a sub-mount under the first electrode pad; and
  - a second electrode pad electrically connected to the second electrode,
 wherein the first and second active layers include a well layer and a barrier layer,
 wherein the first and second active layers and the first, second and third electrode contacting layers are formed of a nitride-based semiconductor layer,
 wherein the reflective electrode layer vertically overlaps the first and second active layers,
 wherein the reflective electrode layer is formed of a different metal from a metal of the conductive support member,
 wherein a lateral width of the first electrode pad is greater than a lateral width of the reflective electrode layer,
 wherein the first electrode is electrically connected to the first electrode pad, and
 wherein both the first electrode pad and the second electrode pad are disposed on a top surface of the sub-mount.
2. A semiconductor light emitting device comprising:
  - a first electrode contacting layer comprising a first semiconductor layer and a second semiconductor layer, the first and second semiconductor layers formed of a p-type nitride-based semiconductor layer, the second semiconductor layer being disposed under the first semiconductor layer;
  - a plurality of active layers disposed between the first and second semiconductor layers;
  - a second electrode contacting layer between the plurality of active layers and including an n-type nitride-based semiconductor layer;
  - a second electrode physically contacting the first electrode contacting layer;

9

a first electrode disposed on the first semiconductor layer;  
 a reflective electrode layer disposed under the second semiconductor layer;  
 a conductive support member disposed under the reflective electrode layer;  
 a first electrode pad under the conductive support member;  
 a sub-mount under the first electrode pad; and  
 a second electrode pad electrically connected to the second electrode,  
 wherein the plurality of active layers include a well layer and a barrier layer,  
 wherein the plurality of active layers are formed of a nitride-based semiconductor layer,  
 wherein the reflective electrode layer vertically overlaps the plurality of active layers,  
 wherein the reflective electrode layer is formed of a different metal from a metal of the conductive support member,  
 wherein a lateral width of the first electrode pad is greater than a lateral width of the reflective electrode layer,  
 wherein the first electrode is electrically connected to the first electrode pad, and  
 wherein both the first electrode pad and the second electrode pad are disposed on a top surface of the sub-mount.

3. The semiconductor light emitting device according to claim 1, wherein each of the first and second active layers includes an InGaN well layer and a GaN-based barrier layer.

4. The semiconductor light emitting device according to claim 2, wherein the plurality of active layers includes the well and barrier layers having a same cycle within each active layer.

5. The semiconductor light emitting device according to claim 1, further comprising a first wire connected to the first electrode and a second wire connected to the second electrode.

6. The semiconductor light emitting device according to claim 1, wherein the well layer of the first active layer is formed of a same semiconductor material as the well layer of the second active layer, and

wherein the well and barrier layers of the first active layer have a same cycle as a cycle of the well and barrier layers of the second active layer.

10

7. The semiconductor light emitting device according to claim 3, wherein the well and barrier layers of the first active layer have a same cycle as a cycle of the well and barrier layers of the second active layer.

8. The semiconductor light emitting device according to claim 1, wherein the first and third electrode contacting layers are electrically connected to the first electrode pad.

9. The semiconductor light emitting device according to claim 1, wherein the conductive support member includes at least one of Cu and Au and the reflective electrode layer includes at least one of Al, Ag, Pd and Pt.

10. The semiconductor light emitting device according to claim 2, wherein the first semiconductor layer and the second semiconductor layer are electrically connected to the first electrode pad.

11. The semiconductor light emitting device according to claim 2, wherein the conductive support member includes at least one of Cu and Au and the reflective electrode layer includes at least one of Al, Ag, Pd and Pt.

12. The semiconductor light emitting device according to claim 1, wherein the lateral width of the reflective electrode layer is greater than a lateral width of the second active layer.

13. The semiconductor light emitting device according to claim 2, wherein the plurality of active layers comprises a first active layer on the first electrode contacting layer and a second active layer on the second electrode contacting layer, wherein the first active layer is on the second semiconductor layer, and

wherein the lateral width of the reflective electrode layer is greater than a lateral width of the second active layer.

14. The semiconductor light emitting device according to claim 1, wherein a bottom surface of the first electrode pad is flush with a bottom surface of the second electrode pad.

15. The semiconductor light emitting device according to claim 2, wherein a bottom surface of the first electrode pad is flush with a bottom surface of the second electrode pad.

16. The semiconductor light emitting device according to claim 5, wherein the first electrode is directly connected to the first electrode pad by the first wire.

17. The semiconductor light emitting device according to claim 2, further comprising a first wire directly connecting the first electrode to the first electrode pad.

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